Integrated circuits improved the quality of human life in evolutionary and revolutionary ways by providing smart devices with internet access and electronic equipment with huge computing power. One of the emerging trends of integrated circuits is to apply the technology toward the smarter society, which drastically improves the quality of life of people with the aid of mass-producible electronic devices equipped with high performance & low power integrated circuits. Sensors, RF and analog circuits, data converters, and digital signal processing circuits will be required to implement the smart mobile devices which enable high-quality human life. State-of-the-art R&D results will be presented in the conference.

**Plenary Talks (Nov. 13–14)**

9:20-10:05, Nov. 13
“Expectations for the Semiconductor Technologies in EVs and HVs”
Dr. Shoichi Sasaki
Professor, Keio Univ. Japan

10:05-10:50, Nov. 13
“Semiconductor Memory Scaling and Beyond”
Dr. Sungjoo Hong
SVP, SK hynix Inc. Korea

9:00-9:45, Nov. 14
“Integrated Circuits and Systems toward Smart Ubiquitous Patient-Centered Medical Environment”
Dr. Ming-Fong Chen
Superintendent, NTU Hospital, Taiwan

9:45-10:30, Nov. 14
“Technology Challenges and Opportunities for Ubiquitous Computing”
Dr. Shekhar Borkar
Intel Fellow, Intel Corp. U.S.A.

**Panel Discussions (Nov. 13)**

Disruptive Design for Emerging Technology after 3D Devices/FinFET and Beyond; How Can We Make It?
Organizer: Youngmin Shin, Samsung, Korea, South
Co-organizer: Youngmin Shin, Samsung, Korea, South
Moderator: Toshiro Hiramoto, The University of Tokyo, Japan
Panelists:
- Vinod Kariot, Cadence, Unite States
- Seiichiro Yamaguchi, Fujitsu, Japan
- Aaron Thean, IMEC, Belgium
- Jae Cheol Son, Samsung, Korea, South
- Jung-Ho Lee, Seoul National University, Korea, South
- Philippe Magarshack, STMicroelectronics, France
- Sally Liu, TSMC, Taiwan

Challenge for Zero Stand-by Power Management – Road-map to the “Normally-Off Computing” –
Organizer: Kazutami Arimoto, Okayama Prefecture Univ., Japan
Co-organizer: Toru Shimizu, Renesas Electronics, Japan
Moderator: Hiroshi Nakamura, The University of Tokyo, Japan
Panelists:
- S. Fujita, Toshiba, Japan
- H. J. Yoo, KAIST, Korea, South
- M. Hayashikoshi, Renesas Electronics, Japan
- H. Takada, Nagoya University, Japan
- Steven Bartling, Texas Instruments, United States
- TBD, IMEC, Belgium
- Shey-shi, National Taiwan University, Taiwan

**Technical Sessions (Nov. 13–14)**

- Analog Interfaces and Amplifiers
- Advanced Memory
- TX/RX Architecture and Building Blocks
- Energy Efficient Circuits and Techniques
- High-Speed Transceivers and Building Blocks
- Nyquist-Rate ADCs
- Emerging Biomedical Circuits and Systems
- Low-Power Digital Communication and Multimedia SoCs
- Power Management ICs
- Oversampling ADCs
- Millimeter-Wave Circuits and Systems
- Clock Generation and Timing Circuits
- SSD Memory and High Frequency Analog
- Ultra Low-Power Circuits for Emerging Communication Systems
- VCO and PLL
- Low-Power SoCs and Circuits

**Tutorials (Nov. 12)**

1. SoC Power Reduction and Management Techniques
   Stefan Rusu, Intel

2. Designing CMOS Wireless LAN System-on-a-Chip
   Srenik Mehta, Qualcomm Atheros

3. High Performance SRAM Design in Deep Nanometer Technologies
   Jente B Kuang, IBM

4. Smart Sensor Design in Standard CMOS
   Kofi Makinwa, Delft Univ. of Technology

**Industry Sessions (Nov. 13)**

1. Leading Edge SoCs and Memory
2. Energy Efficient Circuits for Emerging Applications

Early-bird registration is due on September 16

Online registration is available at:
http://www.a-sscc2012.org/
### A-SSCC 2012 Program at a Glance

**Monday, November 12**

**9:30–12:25 Tutorial I:**
**SoC Power Reduction and Management Techniques**
Srenik Mehta, Qualcomm Atheros

CMOS process technology scaling has enabled higher feature integration in system-on-chip with multiple CPU and graphics cores and larger on-die caches. Reducing and managing power consumption is the most challenging task in today's highly complex systems. In this tutorial, we will review power reduction and management techniques implemented in recent microprocessor and SoC designs, covering the entire spectrum from server to handheld applications. We will review flip-flop power optimization techniques, clock loading reduction, low-voltage operation, leakage reduction techniques, dynamic voltage and frequency scaling, and fine-grain power management techniques. Special attention will be devoted to adaptive circuit techniques that reduce the voltage and frequency design guard-bands. This tutorial includes recent innovations and practical examples from both industry and academic research.

**13:25–16:20 Tutorial III:**
**High Performance SRAM Design in Deep Nanometer Technologies**
Jente B Kuang, IBM

Multi-core processors demand larger on-die memories in order to maximize system performance. Further, continued scaling of the CMOS devices is being enabled through technological advancements such as fully depleted SOI, high-K metal gate, FinFETs with double gate and even further, three-dimensional circuits are being utilized to push the frontiers of high-performance circuits. All of these technological advancements present unique sets of challenges to high performance memory design. This tutorial discusses trends and challenges in high performance SRAM design in deep nanometer technologies including memory designs across high performance and energy efficiency spectrum, assist circuits, reliability and memory design in eXa-scale era.

**13:25–16:20 Tutorial IV:**
**Smart Sensor Design in Standard CMOS**
Prof. Kofi Makinwa, Delft University of Technology

Smart sensors are everywhere! They can be found in our homes, our cars and in nearly all mobile phones. However, processing weak sensor signals is quite challenging, especially when it must be done in standard CMOS, whose precision is limited by 1/f noise, and with severe pin counts and power consumption. In this tutorial, basic circuit techniques to push the frontiers of high-performance circuits will be presented. The use of ultra-low-power SoCs, whose precision is limited by 1/f noise, component tolerances and mismatch. In this tutorial, a system approach to the design of smart sensors will be presented. The use of dynamic techniques, such as chopping, auto-zeroing, dynamic element matching and Δ modulation, to trade off precision versus speed will be discussed. Examples will be given of state-of-the-art CMOS smart sensors for the measurement of temperature, humidity, magnetic field and even wind velocity.

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### A-SSCC 2012 Tutorial I-Monday, November 12

**9:30–12:25 Tutorial I: SoC Power Reduction and Management Techniques**
Srenik Mehta, Intel

Wireless LAN SoCs are ubiquitous today in mobile, computing, and consumer electronics. The simultaneous push for low-cost and high-performance has necessitated the use of scaled CMOS technology with extensive use of digital calibration. This tutorial provides an overview of the challenges in designing CMOS wireless LAN System-on-a-Chip from the perspective of an analog designer. An overview of transceiver building blocks, integration issues, and calibration techniques are described. Two system-on-a-chip examples are presented to contrast the techniques required for low-cost highly integrated 1x1 WLAN SoC versus a high-performance 3x3 WLAN SoC.

Jente B Kuang, IBM

Multi-core processors demand larger on-die memories in order to maximize system performance. Further, continued scaling of the CMOS devices is being enabled through technological advancements such as fully depleted SOI, high-K metal gate, FinFETs with double gate and even further, three-dimensional circuits are being utilized to push the frontiers of high-performance circuits. All of these technological advancements present unique sets of challenges to high performance memory design. This tutorial discusses trends and challenges in high performance SRAM design in deep nanometer technologies including memory designs across high performance and energy efficiency spectrum, assist circuits, reliability and memory design in eXa-scale era.

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Prof. Kofi Makinwa, Delft University of Technology

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Jente B Kuang, IBM

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**http://www.a-sscc2012.org/**
9:20 - 10:50 Plenary Session 1

Tuesday, November 13

11:00-12:45 Industry Session 1: Leading Edge SoCs and Memory

12:20 A Low-Power 6.6-Gb/s Wireline Transceiver for Low-Cost Phones
J. Van Rethy, H. Danneels, V. De Smedt, W. Dehaene, G. Gielen

11:55 A High Performance 64Gb MLC NAND Flash Memory in 20nm CMOS
J. Choi, H. Chung, J. Kim, E. Jang, C. Lee

11:30 Circuit Design Challenges and Solutions for Optical Ring Modulators

11:05 0.5V Start-Up 0.77mm2 Dual Drive Mode on-Chip Single-Inductor Dual-Output (SIDO) DC–DC Boost Converter for Battery and Solar Cell Operation Portable Equipments

10:05 Plenary Talk 2: Semiconductor Memory Scaling and Beyond
Dr. Sungjoo Hong

Tuesday, November 13

13:45-15:50 Session 4: Energy Efficient Circuits and Techniques

14:10 A Power-Efficient All-Digital IR–UWB Transmitter with Configurable Pulse Shaping by Utilizing a Digital Amplitude Modulation Technique
S. Geng(2), X. Chen(2), W. Rheel(2), J. Kim(1), D. Kim(1), Z. Wang(2)
[1]Samsung Advanced Institute of Technology, Korea, South; [2]Nanyang Technological University, Singapore

14:35 A 250-MHz 18-Bit Full Ternary Cam with Low Voltage Match Line Sense Amplifier in 65nm CMOS
Y. Sinagil, A. Chandrakasan

14:00 An Embedded Energy Monitoring Circuit for a 128kbit SRAM with Body–biased Sense-Amplifiers
M. Shirata, S. Morizane, K. Dosaka, K. Nii, H. Noda, H. Kawai

13:45 Adaptive Program Verify Scheme for Improving NAND Flash Memory Performance and Lifespan
S. Park(1), D. Shin(2)
[1]Samsung Electronics, Korea, South; [2]Sungkyunkwan University, Korea, South

13:45 A 0.25V 16Mb Full Ternary Cam with Latchup Resistant and Programmable Accuracy
J. Min, G. Hwang, W. Park, D. Kim

13:35 A 250–MHz 18–Mb Full Ternary Cam with Low Voltage Match Line Sense Amplifier in 65nm CMOS

13:45 Adaptive Program Verify Scheme for Improving NAND Flash Memory Performance and Lifespan
S. Park(1), D. Shin(2)
[1]Samsung Electronics, Korea, South; [2]Sungkyunkwan University, Korea, South

13:40 An Efficient BCH Decoder with 124-Bit Correctability for Multi–Channel SSD Applications
H. Tsai, C. Yang, H. Chang
National Chiao Tung University, Taiwan

13:35 A 250MHz 18-Bit Full Ternary Cam with Low Voltage Match Line Sense Amplifier in 65nm CMOS

13:30 Circuit Design Challenges and Solutions for Optical Ring Modulators

13:05 A 0.5V 10MHz–to–100MHz 0.47uW/MHz Power Scalable AD–PLL in 40nm CMOS
Y. Hirakawa(2), J. Hayashi(2), H. Chung(1), T. Kuroda(1), H. Ishikuro(1)
[1]Keio University, Japan; [2]Semiconductor Technology Academic Research Center, Japan

12:20 A Low-Power 6.6–Gb/s Wireline Transceiver for Low-Cost FPGAs in 28nm CMOS
J. Savoj, K. Hsiao, F. An, M. Buckley, J. Im, X. Jiang, A. Jose, V. Kireev, K. Lai, H. Pham, D. Turker, D. Wu, K. Chang

12:05 Circuit Design Challenges and Solutions for Optical Ring Modulators

11:55 A 0.5V 10MHz–to–100MHz 0.47uW/MHz Power Scalable AD–PLL in 40nm CMOS
Y. Hirakawa(2), J. Hayashi(2), H. Chung(1), T. Kuroda(1), H. Ishikuro(1)
[1]Keio University, Japan; [2]Semiconductor Technology Academic Research Center, Japan

11:30 A 1.94mm2, 38.17mW Dual VP8/H.264 Full-HD Encoder/Decoder LSI for Social Network Services (SNS) Over Smart-Phones
D. Han, Y. Zheng

11:05 The First 22 nm IA System-on-Chip Using tri-Gate Transistors
S. Siers

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A-SSCC 2012 Program Schedule – Tuesday, November 13 & Wednesday, November 14

**Tuesday, November 13**

13:45–15:50  Session 4: Energy Efficient Circuits and Techniques (Continued)

G. Ocho, M. Diva, M. Nakayama, Y. Kanno
Hitachi, Japan

15:00 Monitoring Effective Supply Voltage Within Power Rails of Integrated Circuits
T. Okumoto, K. Yoshikawa, M. Nagata
Kobe University, Japan

15:25 A 0.3-V All Digital Crystal–Less Clock Generator for Energy Harvester Applications
J. Liu[1], W. Lee[1], H. Huang[3], K. Cheng[2], C. Huang[1], Y. Liang[1], J. Peng[1], Y. Chui[1]
[1]Industrial Technology Research Institute
[2]National Central University, Taiwan;
[3]National Taipei University, Taiwan

16:05–17:45 Panel Discussion 1: Disruptive design for emerging technology after 3D Devices/FinFET and beyond: How can we make it?
Organizer: Yung-Chow Peng, TSMC, Taiwan
Co-organizer: Yoonmin Shin, Samsung, Korea, South
Moderator: Toshiro Hiramoto, The University of Tokyo, Japan
Panelist: Vind Kariat, Cadence, United States
Seichiro Yamaguchi, Fujitsu, Japan
Aaron Thean, IMEC, Belgium
Jae Cheol Son, Samsung, Korea, South
Jong–Hu Lee, Seoul National University, Korea, South
Philipp Maqarshack, STMicroelectronics, Korea
Sally Liu, TSMC, Taiwan

16:05–17:45 Panel Discussion 2: Challenge for Zero Stand-by Power Management – Road-map to the “Normally-Off Computing”
Organizer: Kazutami Arimoto, Okayama Prefecture University, Japan
Co-organizer: Toru Shimizu, Renesas Electronics, Japan
Moderator: Hiroshi Nakamura, The University of Tokyo, Japan
Panelist: S. Fujita, Toshiba, Japan
H. J. Yoo, KAIST, Korea, South
M. Hayashikoshi, Renesas Electronics, Japan
H. Takada, Nagoya University, Japan
Sh. Jen Bartling, Texas Instruments, United States
TBD, IMEC, Belgium
Shy–shi, National Taiwan University, Taiwan

18:00–20:00 Banquet

**Wednesday, November 14**

09:00–10:30 Plenary Session 2
09:00 Plenary Talk 3: Integrated Circuits and Systems toward Smart Ubiquitous Patient–Centered Medical Environment
Dr. Ming–Chang Shen
Superintendent, NTU Hospital, Taiwan

09:45 Plenary Talk 4: Technology Challenges and Opportunities for Ubiquitous Computing
Dr. Shekhar Borkar
Intel Fellow, Intel, United States

10:45–12:50 Session 5: High Speed Transceivers and Building Block (Continued)

10:45 A 20Gb/s Adaptive Dubioline Transceiver
S. Liu, I. Lee, Y. Ying
National Taiwan University, Taiwan

11:10 A 2.3–mW, 5–Gb/s Decision–Feedback Equalizing Receiver Front–End with Static–Power–Free Signal Summation and CDR–Based Precursor ISI Reduction
S. Son, H. Kim, M. Park, K. Kwon, J. Kim
Seoul National University, Korea, South

11:35 A 24–Gb/s Source–Series Terminated Driver with Inductor Peaking in 28–nm CMOS
Fujitsu Laboratories, Japan

12:00 A 5 Gb/s 1/4–Rate Clock and Data Recovery Circuit Using Dynamic Stepwise Bang–Bang Phase Detector
Y. Lee[2], S. Chang[2], R. Chiu[2], Y. Lin[2], Y. Chen[2], J. Goh[2], C. Huang[1]
[1]Himax Technologies, Inc., Taiwan;
[2]National Cheng–Kung University, Taiwan

12:25 A 0.1–1.5 GHz 8–bit Inverter–Based Digital–to–Phase Converter Using Harmonic Rejection
M. Chen, A. Hafez, C. Yang
UCLA, United States

10:45–12:50 Session 6: Nyquist–Rate ADCs
10:45 A 1–Ghz, 17.5–mW, 8–bit Subranging ADC Using Offset–Cancelling Charge–Steering Amplifier
K. Ohhata, H. Takase, M. Tatoe, M. Arita, N. Imakake, Y. Yonemitsu
Kaposhima University, Japan

10:55 Inter–Stage Gain Error Self–Calibration of a 31.50 10b 470MS/s Pipelined–SAR ADC
Z. Jiaoyu, Z. Yan, S. Sai Weng, U. Seng Pan, M. Rui Paulo
Univ. of Macau, Shih, Singapore, China

11:25 A 12–Bit 8.47–fj/Conversion–Step 1–MS/s SAR ADC Using Capacitor–Swapping Technique
M. Wu, Y. Chung, H. Li
MediTek, Taiwan

11:45 A 40nm CMOS Full Asynchronous Nano–Watt SAR ADC with 98% Leakage Power Reduction by Boosted Self Power Gating
R. Sekimoto, A. Shikata, Y. Koshikita, T. Kuroda, H. Ishikuro
Keio University, Japan

12:05 A 0.05mm2 0.6V 500ks/s 1.438 Conversion–Step 11–Bit Two–Step Switching SAR ADC for 3–Dimensional Stacking CMOS Image
J. Lin[2], H. Huang[2], C. Hsieh[2], H. Chen[1]
[1]Industrial Technology Research Institute, Taiwan;
[2]National Tsing Hua University, Taiwan

12:25 A 9b 1GS/s 27mW Two–Stage Pipeline ADC in 45nm SOI–CMOS
P. Pennillo[1], M. Flynn[2]
[1]University of Michigan, United States;
[2]University of Michigan, United States

10:45 – 12:50 Session 7: Emerging Biomedical Circuits and Systems
10:45 Ultrasonic Imaging Front–End Design for CMUT: a 3–Level 30Vpp Pulse–Shaping Pulser with Improved Efficiency and a Noise–Optimized Receiver
K. Chen, A. Chandraksan, C. Codini
MIT, United States

J. Cheong[1], C. Heo[1], S. Ng[1], R. Xue[1], H. Cha[2], P. Khannur[1], X. Liu[1], A. Lee[1], W. Park[2], L. Lim[1], C. He[1], M. Je[1]
[1]Institute of Microelectronics, A–STAR (Agency for Science, Technology and Research), Singapore;
[2]Nanyang Technological University, Singapore; {3}National University of Singapore, Singapore

11:35 An Inductively Powered CMOS Multichannel Bionic Neural Link for Peripheral Nerve Function Restoration
K. Ng[3], X. Liu[3], J. Zhao[3], S. Yen[3], Y. Xu[3], T. Tan[3], M. Je[1]
[1]Institute of Microelectronics, A–STAR (Agency for Science, Technology and Research), Singapore;
[2]Seoul National University of Science and Technology, Korea, South

12:00 100–Channel Wireless Neuro Recording System with 54–Mb/s Data Link and 40%–Efficiency Power Link
M. Je[1], K. Cheng[1], X. Zou[1], J. Cheong[1], R. Xue[1], Z. Chen[1], L. Yao[1], H. Cha[2], S. Cheng[1], P. Li[1], L. Liu[2], L. Andia[1]
[1]Institute of Microelectronics, A–STAR (Agency for Science, Technology and Research), Singapore;
[2]Nanyang Technological University, Singapore

12:25 A Dynamic Impedance Matched Acupuncture–Type Diagnosis System with Concurrent Feedback of Physiological Signals
K. Song, S. Hong, T. Roh, U. Hoo, H. Yoo
KAIST, Korea, South

12:37 A Single–Chip Time–Interleaved 32–Channel Analog Beamformer for Ultrasound Medical Imaging
J. Um, J. Kim, E. Song, Y. Kim, J. Sim, H. Park
POSTECH, Korea, South

http://www.a-sscc2012.org/
Wednesday, November 14
10:45-12:50 Session 8: Low-Power Digital Communication and Multimedia SoCs
10:45 A 40 nm 535 Mb/s Multiple Code-Rate Turbo Decoder Chip Using Reciprocal Dual Trellis C. Lin, C. Wong, H. Chang National Chiao Tung University, Taiwan
11:10 First (50,2,4) Nonbinary LDPC Convolutional Code Decoder Chip Over GF(2^56) in 90nm CMOS C. Lin, C. Chen, H. Chang, C. Lee National Chiao Tung University, Taiwan
12:25 A Dynamic Resource Controller with Network-on-Chip for a 10.5nJ/Pixel Object Recognition Processor J. Oh, H. Hong, G. Kim, J. Park, H. Yoo KAIST, Korea, South
12:37 An 800MHz Cryptographic Pairing Processor in 65nm CMOS Y. Li, J. Han, S. Wang, D. Fang, X. Zeng Fudan University, China
13:00-15:55 Session 9: Power Management ICs
13:50 A Package Bondwire Based 80% Efficiency 80MHz Fully-Integrated Buck Converter with Precise DCM Operation and Enhanced Light-Load Efficiency C. Huang, P. Mol The Hong Kong University of Science and Technology, Hong Kong
14:40 Automatic Loading Detection (ALD) Technique for 92% High Efficiency Interleaving Power Factor Correction (PFC) Over a Wide Output Power of 180W J. Tsai National Chiao Tung University, Taiwan, Taiwan
15:05 A Chip–Area–Efficient CMOS Low-Dropout Regulator Using Wide-Swing Voltage Buffer with Parabolic Adaptive Biasing for Portable Applications Y. Liu, C. Zhan, L. Cheng, W. Ki HKUST, Hong Kong
15:30 A Low–Power and Low–Cost Digitally–Controlled Boost LED Driver IC for Backlights T. Oh, A. Cho, S. Ki, I. Hwang Kangwon National University, Korea, South
13:00-15:55 Session 10: Oversampling ADCs
14:15 A 7.5mW 9 MHz CT ΔΣ Modulator in 65 nm CMOS with 69 dB SNDR and Reduced Sensitivity to Loop Delay Variations M. Andersson[1], M. Anderson[1], L. Sundström[1], P. Andreasson[2] Ericsson AB, Sweden, [2]Lund University, Sweden
15:30 A 0.8 V 80.3 dB SNDR Stage–Shared ΔΣ Modulator with Chopper–Embedded Switched–Opamp for Biomedical Application C. Hsiao, W. Chen, C. Hsieh National Tsing Hua University, Taiwan
13:00-15:55 Session 11: Millimeter Wave Circuits and Systems
13:00 A 245 GHz, 2.6mW/Pixel Antenna–Less CMOS Imager with 0.77W/Hz^0.5 Nef and 3.5m Backscattered Range A. Tang, H. Wu, F. Chang UCLA, United States
14:15 A 34.8%–PAE CMOS Transmitter Frontend for 24–GHz FMCW Radar Applications H. Chen, L. Lu National Taiwan University, Taiwan
13:50 A 0.7V–to–1.0V 10.1 dBm–to–13.2 dBm 60–GHz Power Amplifier Using Digitally-Assisted LDG Considering HCI Issue R. Wu, Y. Tsukui, R. Minami, K. Okada, A. Matsuzawa Tokyo Institute of Technology, Japan
15:05 A 60 GHz Wideband Active Balun Using Magnitude and Phase Current Correction Technique in 65nm CMOS S. Chou, F. Huang, C. Wang National Taiwan University, Taiwan
15:30 A 60GHz VCO with 25.8% Tuning Range by Switching Return Path in 65nm CMOS W. Fei, H. Yu, K. Yeo, W. Lim Nanyang Technological University, Singapore
15:42 A 60GHz CMOS Rectifier with ~27.5dBm Sensitivity for mm–Wave Power Detection S. Kawai, T. Mitomo, S. Saigusa Toshiba, Japan
13:00–15:55 Session 12: Clock Generation and Timing Circuits
13:50 A Spread Spectrum Clock Generator Using Phase/Frequency Boosting with a Peak Power Reduction 14.6dB, RMS jitter 1.45ps and Power 4.8mW/ GHz for USB 3.0 Y. Choi, S. Jeon, B. Ki, J. Kim, H. Park POSTECH, Korea, South
14:15 A Multi–Phase Multi–Frequency Clock Generator Using Superharmonic Injection Locked Multithin Ring Oscillators As Frequency Divider A. Hafez, M. Chen, K. Yang UCLA, United States
14:40 A High–Resolution Wide–Range Dual–Loop Digital Delay–Locked Loop Using a Hybrid Search Algorithm J. Kim, S. Han Hongik University, Korea, South
15:05 An All–Digital Phase–Locked Loop with Dynamic Phase Control for Fast Locking Y. Huang, S. Tsai, C. Liu, T. Lin National Taiwan University, Taiwan
15:30 A Cint–Less Type–II PLL with ΔΣ DAC Based Frequency Acquisition and Reduced Quantization Noise Z. Zhang, K. Chen, W. Rhee, Z. Wang Tsinghua University, China
15:42 Delay–Line Based Fast–Locking All–Digital Pulsedwidth–Control Circuit with Programmable Duty Cycle J. Su, T. Liao, C. Hung National Chiao Tung University, Taiwan
A-SSCC 2012 Program Schedule – Wednesday, November 14

16:10 – 18:15 Session 13: SSD Memory and High Frequency Analog
16:10 Vset/Reset and Vpgm Generator Without Boosting Dead Time for 3D-REAM and NAND Flash Hybrid Solid-State Drives
   T. Harada{1}, K. Takeuchi{1}
   {1}Chuo University, Japan
16:15 An Integrated Variable Positive/Negative Temperature Coefficient Read Reference Generator for MLM PCM/NAND Hybrid 3D SSD
   K. Miyaji{1,2}, K. Higuchi{1,2}, T. Takeuchi{1}
   {1}Chuo University, Japan; {2}University of Tokyo, Japan
17:00 A 5.6GHz Digital Arbitrary Phase-Setting Type II PLL in 65nm CMOS with 2.23deg Resolution
   L. Li{1}, M. Ferretti{1}, M. Flynn{2}
   {1}IBM T. J. Watson Research Center, United States; {2}University of Michigan, United States
17:25 A 0.5V GFSK 200μW Limiter/Demodulator with Bulk-Driven Technique for Low-IF Bluetooth
   C. Lai, M. Shen, Y. Wu, P. Huang
   National Taiwan University, United States
17:50 Wireless Wafer Probing for on-Chip Analog Voltage Measurement
   D. Lee, D. Wentzloff, J. Hayes
   University of Michigan, United States
16:10 Photovoltaic-Assisted CMOS Rectifier Circuit for Synergistic Energy Harvesting from Ambient Radio Wave
   K. Kotani, T. Bando, Y. Sasaki
   Tohoku University, Japan
   J. Bae, H. Eshita, K. Aihara
   KAIST, Korea, South
17:00 A 2.4/5.8 GHz 10 μW Wake-Up Receiver with −65/−50 dBm Sensitivity and Direct Active RF Detection
   K. Cheng{2}, X. Liu{1}, M. Je{1}
   {1}Institute of Microelectronics, Singapore; {2}National Cheng Kung University, Taiwan
17:25 An Asymmetrical QPSK/8QAM Transceiver SoC and 15:1 JPEG Synthesizer Using Fractional-N Injection-Locked Technique
   Y. Gao{2}, S. Cheng{2}, Y. Zhu{1}, W. Liu{1}, X. Liao{1}, M. Je{1}
   {1}Institute of Microelectronics, Singapore; {2}Institute of Infocomm Research, ASTAR, Singapore
17:50 A QPSK/16-QAM OFDM-Based 2.5Mbps LINC Transmitter for Body Channel Communication
   P. Tsai{1}, J. Chang{1}, C. Chen{1}, C. Lee{2}
   {1}MediaTek, Taiwan; {2}National Chiao-Tung University, Taiwan
18:02 Continuous-Time High-Precision IR-UWB Ranging System in 90 nm CMOS
   S. Sudalaiyandi, H. Hjortland, T. Vu, Ø. Næss, T. Lande
   University of Oslo, Norway
16:10 – 18:15 Session 15: VCO and PLL (Continued)
17:25 Heterogeneous Coupled Ring Oscillator Arrays for Reduced Phase Noise at Lower Power Consumption
   P. Dubey{2}, D. Belot{2}, S. Chatterjee{1}
   {1}IIT Delhi, India; {2}STMicroelectronics, France
17:50 A Low Voltage Sub 300μW 2.5GHz Current Reuse VCO
   M. Taghivand{1}, M. Chahraman{1}, M. Aghababaei{2}
   {1}Stanford University, Qualcomm Atheros, United States; {2}University of Michigan, United States
18:02 A 4GHz Locking Range and 0.19 ps Low-Energy Differential Dual-Modulus 10/11 Preascaler
   T. Mitusaka{2}, M. Yamanoue{2}, K. Iizuka{2}, M. Fujishima{1}
   {1}Hirosima University, Japan; {2}SHARP, Japan
16:10 – 18:15 Session 16: Low-Power SoCs and Circuits
16:10 Real-Time Instruction-Cycle-Based Dynamic Voltage Scaling (iDVS) Power Management for Low-Power Digital Signal Processor (DSP) with 53% Energy Savings
   S. Peng
   National Chiao Tung University, Taiwan
16:35 Ultra-Low-Energy Near-Threshold Biomedical Signal Processor for Versatile Wireless Health Monitoring
   X. Liu, J. Zhou, X. Liao, C. Wang, J. Luo, M. Madihan, M. Je
   Institute of Microelectronics, Singapore
17:00 Performance and Side-Channel Attack Analysis of a Self-Synchronous Montgomery Multiplier Processing Element for RSA in 40nm CMOS
   B. Devlin{2}, H. Ueki{1}, S. Morii{1}, S. Miyashita{1}, M. Ikeda{2}, K. Akada{2}
   {1}Renesse Electronics, Japan; {2}The University of Tokyo, Japan
17:25 A Body Bias Generator Compatible with Cell-Based Design Flow for Within-Die Variability Compensation
   N. Kamae, A. Tsuchiya, H. Onodera
   Kyoto University, Japan
17:50 Self-Test Methodology and Structures for Pre-Bond TSV Testing in 3D-IC System
   C. Wang, J. Zhou, B. Zhao, X. Liu, M. Je
   Institute of Microelectronics, Singapore

Registration Fee (Japanese Yen)

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<th>Type</th>
<th>Early-Bird</th>
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<th>On-site Registration</th>
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<tr>
<td>IEEE Regular</td>
<td>45,000</td>
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- Additional Tutorial Book: 4,000
- Additional Proceedings (CD-R only): 2,500

Tutorials
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  - Two Sessions: 16,000
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### Supporter’s Exhibition (Nov. 13 – 14)

<table>
<thead>
<tr>
<th>Affiliation</th>
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<tr>
<td>Agilent Technologies Japan Ltd.</td>
<td>Communication with foundry is very important for circuit designer. Which process is the best for my circuit? How the simulation model is accurate in the range of L, W and temp? But there is no good tool to communicate each other, before. MQA is the golden standard communication tool between foundry and circuit designer. Over 100 company have already use MQA. And Agilent EESof EDA has many circuit design solution in ADS, GoldenGate and SystemVue, Fast Yield Contributor, Circuit Validation with real modulated signal, EM simulation on Virtuoso.</td>
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<td>ATRENTA K.K.</td>
<td>Atrenta’s SpyGlass® Predictive Analysis software platform significantly improves design efficiency for the world’s leading semiconductor and consumer electronics companies. More than two hundred companies and thousands of design engineers worldwide rely on SpyGlass to reduce risk and cost before traditional EDA tools are deployed. Atrenta will be showing how SpyGlass addresses issues such as lint, power, clock synchronization, constraints, testability and routing congestion in their booth.</td>
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<tr>
<td>Mentor Graphics Japan Co., Ltd.</td>
<td>Mentor Graphics® is a leader in electronic design automation software. Our innovative products and solutions help engineers conquer design challenges in the increasingly complex worlds of board and chip design. At A-SSCC 2012, we demonstrate our new D2S backend solutions which are Pyxis products as our analog design environment tools, Olympus-SoC as our P&amp;R tool, Calibre products as our physical verification tools and Tessent products as our test solution tools.</td>
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<tr>
<td>MIPS Technologies</td>
<td>MIPS Technologies as the leading microprocessor IP vendor will introduce the trend of the latest microprocessor technologies including our new and the industry’s most efficient Aptiv(TM) microprocessor cores.</td>
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<td>NEC Corporation</td>
<td>CyberWorkBench and EMIStream have been developed by NEC over the course of twenty years. CyberWorkBench is a C-based LSI design platform developed around the ‘All-in-C’ paradigm that allows high level synthesis and verification of any ANSI-C or SystemC program generating high quality RTL. EMIStream is a PCB level EMI suppression support tool that can suppress undesirable EMI generated from PCB at an early design stage with EMI Design Rule Check and Power Plane Resonance Analysis features. For more information, visit us at <a href="http://www.cyberworkbench.comwww.emistream.com">www.cyberworkbench.comwww.emistream.com</a></td>
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<tr>
<td>OneSpin Solutions Japan K.K.</td>
<td>As the EDA provider with the broadest range of verification products, OneSpin Solutions GmbH is uniquely equipped to handle the verification requirements of both IC and FPGA designers. The technologies employed in OneSpin’s products enable the designer to completely verify their designs, not to only check for specific behaviors. OneSpin representatives will be at A-SSCC to meet with designers in search of verification solutions utilizing formal verification, equivalence checking, advanced linting, and verification coverage analysis.</td>
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<td>Renesas Electronics Corporation</td>
<td>Renesas Electronics, the world’s number one supplier of microcontrollers, is a premier supplier of advanced semiconductor solutions including microcontrollers and a broad range of analog and power devices. At A-SSCC2012, Renesas will present the leading-edge low power MCU technology for smart equipments and demonstrate a unique solution “Smart Analog” for sensor applications.</td>
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<td>ROHM Co., Ltd.</td>
<td>TBD</td>
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<tr>
<td>Semiconductor Technology Academic Research Center (STARC)</td>
<td>Semiconductor Technology Academic Research Center (STARC) was founded in December 1995 with investment from leading Japanese semiconductor companies. STARC will present Company Profile with following activities with academia and industry. - Joint research with universities - Education for LSI design engineers - Prototype fabrication support - Several open program between industry-academia or industry-industry And STARC will especially present summary of Extremely Low Power Project commissioned by METI and NEDO.</td>
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WHERE IN JAPAN:

Kobe is located in Hyogo Prefecture, one of several prefectures in the mid-west of Japan that, together, are known as the ‘Kansai Region’. This is Japan’s premier tourism area for overseas visitors making Kobe an ideal base city for visiting world heritage sites, both to the east and to the west. The Port of Kobe and its man-made islands are located on the north shore of the Osaka Bay.

EASY ACCESS:

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http://kobe-cc.jp/english/access/index.html

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For further information, contact at:
a-sscc2012@semiconportal.com